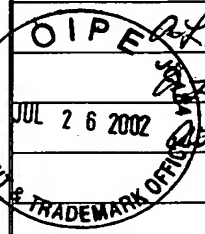



<b>INFORMATION DISCLOSURE CITATION</b>  <b>PTO-1449</b>		ATTY. DOCKET NO. 19329-701		SERIAL NO. 10/029,596			
		APPLICANT Chung-Yang Huang					
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<b>U.S. PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
	5,276,897	1/4/1994	Stalmarck	395	800	6/14/1990	
	5,937,183	8/10/1999	Ashar, et al.	395	500.34	11/5/1996	
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<b>FOREIGN PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
						<input type="checkbox"/>	<input type="checkbox"/>
						<input type="checkbox"/>	<input type="checkbox"/>
						<input type="checkbox"/>	<input type="checkbox"/>
<b>OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)</b>							
07	Chang-Yang (Ric) Huang, et al.; "Using Word Level ATPG and Modular Arithmetic Constraint-Solving Techniques for Assertion Property Checking"; IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20, No. 3, March 2001; pp. 381-391.						
02	Farzan Fallah, et al.; "Functional Vector Generation for HDL models Using Linear Programming and 3-Satisfiability"; Proceedings of 1998 Design Automation Conference; June 15-19, 1998; pp. 528-533						
05	Ranga Vemuri, et al.; "Generation of Design Verification Tests from Behavioral VHDL Programs Using Path Enumeration and Constraint Programming"; IEEE Transactions on Very Large Scale Integration (VLSI) Systems; Vol. 3, No. 2, June 1995; pp. 201-214						
07	"Murphi Description Language and Automatic Verifier"; <a href="http://sprout.stanford.edu/dill/murphi.html">http://sprout.stanford.edu/dill/murphi.html</a> ; November 7, 2001; pp. 1-6						
02	Kenneth L. McMillan; "Symbolic Model Checking"; Kluwer Academic Publishers; 1993						
EXAMINER				DATE CONSIDERED		6/11/03	

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.